IN THE CLAIMS:

Please amend the claims as follows.

1-22. (Cancelled)

23. (New) An apparatus comprising:

a clock encoding circuit configured to receive a source clock signal, wherein the clock encoding circuit is configured to generate an encoded system clock signal using the source clock signal;

a clock decoding circuit including a phase locked loop (PLL), wherein the clock decoding circuit is configured to receive the encoded system clock signal at a first input of the PLL, wherein the clock decoding circuit is configured to generate a phase signal and a core clock signal using the encoded source clock signal; and

a clock generating circuit configured to generate a global clock signal using the phase signal and the core clock signal, and wherein the clock generating circuit is configured to generate a system clock signal that is synchronous with the global clock signal using the encoded clock signal.

24. (New) The apparatus of claim 23, wherein the clock decoding circuit further includes an AND gate, an inverter, and a frequency division circuit, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a first input of the AND gate, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the inverter is coupled between the frequency division circuit and a second input of the AND gate, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL and to the inverter.

25. (New) The apparatus of claim 24, wherein the clock decoding circuit is configured to generate a core clock signal at the output of the PLL and a phase signal at an output of the AND gate.

26. (New) The apparatus of claim 24, wherein the feedback clock signal is the core clock signal divided by two.

27. (New) The apparatus of claim 23, wherein the clock decoding circuit further includes an AND gate, a frequency division circuit, an OR gate, a first inverter, a second inverter, and a third inverter, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a first input of the OR gate, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the first inverter is coupled between the frequency division circuit and a first input of the AND gate, wherein a second input of the OR gate is coupled to the frequency division circuit, wherein the second and third inverters are coupled between an output of the OR gate and a second input of the AND gate, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL, to the first inverter, and to the second input of the OR gate.

28. (New) The apparatus of claim 23, wherein the clock decoding circuit further includes a D flip-flop, an inverter, a time delay circuit, and a frequency division circuit, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a D input of the D flip-flop, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the inverter is coupled between the frequency division circuit and an input of the time delay circuit, wherein an output of the time delay circuit is coupled to a clock input of the D flip-flop, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL and to the inverter.

29. (New) The apparatus of claim 28, wherein the clock decoding circuit is configured to generate a core clock signal at the output of the PLL and a phase signal at an output of the D flip-flop.

30. (New) The apparatus of claim 28, further comprising a plurality of devices, wherein each of the plurality of devices includes a clock decoding circuit and a clock generating circuit.

31. (New) The apparatus of claim 30, wherein the encoded system clock includes additional encoded information, wherein the additional encoded information is state information, a global reset signal, or an identifier for enabling a low power mode.

32. (New) The apparatus of claim 23, wherein the clock encoding circuit includes a first AND gate, a second AND gate, an OR gate, and a frequency division circuit, wherein the clock encoding circuit is configured to receive the source clock signal at an input of the frequency division circuit, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by particular integers.

33. (New) The apparatus of claim 32, wherein the first AND gate is configured to receive a portion of the plurality of signals generated by the frequency division circuit, wherein the second AND gate is configured to receive a remaining portion of the plurality of signals, and wherein the OR gate is configured to receive an output of the first AND gate and an output of the second AND gate and is further configured to generate the encoded system clock signal based on the outputs of the first and second AND gates.

34. (New) The apparatus of claim 32, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by eight, four, two, and one.

35. (New) The apparatus of claim 23, wherein the clock encoding circuit includes a frequency division circuit, a phase shifting delay locked loop (DLL), an AND gate, and an OR

gate, wherein the clock encoding circuit is configured to receive the source clock signal at an input of the frequency division circuit, at an input of the phase shifting DLL, and at a first input of the OR gate, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by particular integers, and wherein the phase shifting DLL is configured to generate a phase shifted source clock signal.

36. (New) The apparatus of claim 35, wherein the AND gate is configured to receive the plurality of signals generated by the frequency division circuit and the phase shifted source clock signal, and wherein the OR gate is configured to receive an output of the AND gate at a second input and is further configured to generate the encoded system clock signal based on the output of the AND gate and the source clock signal.

37. (New) The apparatus of claim 35, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by four and two, and the phase shifting DLL is configured to phase shift the source clock signal by ninety degrees.

38. (New) A computer system comprising:

a clock encoding circuit configured to receive a source clock signal, and wherein the clock encoding circuit is configured to generate an encoded clock signal using the source clock signal; and

a plurality of devices coupled to the clock encoding circuit, wherein each of the plurality of devices includes:

a clock decoding circuit including a phase locked loop (PLL), wherein the clock decoding circuit is configured to receive the encoded system clock signal at a first input of the PLL, wherein the clock decoding circuit is configured to generate a phase signal and a core clock signal using the encoded source clock signal, and

a clock generating circuit configured to generate a global clock signal using the phase signal and the core clock signal, and wherein the clock generating circuit is configured to generate a system clock signal that is synchronous with the global clock signal using the encoded clock signal.

39. (New) The computer system of claim 38, wherein the clock decoding circuit further includes an AND gate, an inverter, and a frequency division circuit, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a first input of the AND gate, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the inverter is coupled between the frequency division circuit and a second input of the AND gate, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL and to the inverter.

40. (New) The computer system of claim 39, wherein the clock decoding circuit is configured to generate a core clock signal at the output of the PLL and a phase signal at an output of the AND gate.

41. (New) The computer system of claim 38, wherein the clock decoding circuit further includes an AND gate, a frequency division circuit, an OR gate, a first inverter, a second inverter, and a third inverter, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a first input of the OR gate, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the first inverter is coupled between the frequency division circuit and a first input of the AND gate, wherein a second input of the OR gate is coupled to the frequency division circuit, wherein the second and third inverters are coupled between an output of the OR gate and a second input of the AND gate, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL, to the first inverter, and to the second input of the OR gate.

42. (New) The computer system of claim 38, wherein the clock decoding circuit further includes a D flip-flop, an inverter, a time delay circuit, and a frequency division circuit, wherein the clock decoding circuit is configured to receive the encoded system clock signal at the first input of the PLL and at a D input of the D flip-flop, wherein the frequency division circuit is coupled between an output of the PLL and a second input of the PLL, wherein the inverter is coupled between the frequency division circuit and an input of the time delay circuit, wherein an output of the time delay circuit is coupled to a clock input of the D flip-flop, and wherein the frequency division circuit is configured to provide a feedback clock signal to the second input of the PLL and to the inverter.

43. (New) The computer system of claim 42, wherein the clock decoding circuit is configured to generate a core clock signal at the output of the PLL and a phase signal at an output of the D flip-flop.

44. (New) The computer system of claim 38, wherein the encoded system clock includes additional encoded information, wherein the additional encoded information is state information, a global reset signal, or an identifier for enabling a low power mode.

45. (New) The computer system of claim 44, wherein if the plurality of devices receive the encoded system clock including state information, at least one of the devices is configured to decode the state information to alter a state of the device.

46. (New) The computer system of claim 38, wherein the clock encoding circuit includes a first AND gate, a second AND gate, an OR gate, and a frequency division circuit, wherein the clock encoding circuit is configured to receive the source clock signal at an input of the frequency division circuit, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by particular integers.

47. (New) The computer system of claim 46, wherein the first AND gate is configured to receive a portion of the plurality of signals generated by the frequency division circuit, wherein the second AND gate is configured to receive a remaining portion of the plurality of signals, and wherein the OR gate is configured to receive an output of the first AND gate and an output of the second AND gate and is further configured to generate the encoded system clock signal based on the outputs of the first and second AND gates.

48. (New) The computer system of claim 38, wherein the clock encoding circuit includes a frequency division circuit, a phase shifting delay locked loop (DLL), an AND gate, and an OR gate, wherein the clock encoding circuit is configured to receive the source clock signal at an input of the frequency division circuit, at an input of the phase shifting DLL, and at a first input of the OR gate, wherein the frequency division circuit is configured to generate a plurality of signals that correspond to the source clock signal divided by particular integers, and wherein the phase shifting DLL is configured to generate a phase shifted source clock signal.

49. (New) The computer system of claim 48, wherein the AND gate is configured to receive the plurality of signals generated by the frequency division circuit and the phase shifted source clock signal, and wherein the OR gate is configured to receive an output of the AND gate at a second input and is further configured to generate the encoded system clock signal based on the output of the AND gate and the source clock signal.